ABSTRACT

A FPGA data module to be referred to as a LUT by a logic block (43) is divided into a plurality of modules. Each of a plurality of data registers (41a to 41d) stores one of the plurality of FPGA data modules. By referring to the FPGA data module(s) stored in one or more of the plurality of data registers (41a to 41d), a gate circuit (43a) and flip flop (43b) of the logic block (43) generates a logical function value of logic input data. The logical function value of the logic input data is provided as logic output data.